

Column-Selection-Enabled 10T SRAM Utilizing Shared Diff-VDD Write and Dropped-VDD Read for Power Reduction

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Abstract—A nondestructive column-selection-enabled 10T SRAM for aggressive power reduction is presented in this brief. It frees a half-selected behavior by exploiting the bitline-shared data-aware write scheme. The differential-VDD (Diff-VDD) technique is adopted to improve the write ability of the design. In addition, its decoupled read bitlines are given permission to be charged and discharged depending on the stored data bits. In combination with the proposed dropped-VDD biasing, it achieves the significant power reduction. The experimental results show that the proposed design provides the 3.3× improvement in the write margin compared with the standard Diff-10T SRAM. A 5.5-kb 10T SRAM in a 65-nm CMOS process has a total power of 51.25 μ W and a leakage power of 41.8 μ W when operating at 6.25 MHz at 0.5 V, achieving 56.3% reduction in dynamic power and 32.1% reduction in leakage power compared with the previous single-ended 10T SRAM.

Index Terms—10T SRAM, bit-interleaving, column selection, differential VDD (Diff-VDD), low-power SRAM, power reduction.

I. INTRODUCTION

The ultralow-voltage operation of digital circuits offers a niche for applications with high constraints on energy efficiency or low power consumption, such as implantable instruments, biomedical devices, and wireless sensors. Compared with other circuits, SRAM has always drawn much more attention in low-voltage regions since it places a restriction on VDD scaling and dominates the major power and performance of the chips.

Traditional 6T SRAM widely used in commercial ICs has been a workhorse for many years. While providing beneficial concerning area efficiency, it is associated with the challenge of read stability and write ability in low-voltage domains toward process, voltage, and temperature variations, thus resulting in the degraded circuit behavior or even failure. The major reason for the V_{DDmin} limitation in 6T SRAM is the contradiction between read and write requirements as well as the direct-read-access mechanism [1].

To realize the low-voltage operation, a superior alternative is the single-ended 8T (SE-8T) SRAM cell [2]. It separates the read path from the cell core by adding an isolated 2T read port, enabling read and write V_{DDmin} s to be capable of optimizing independently. Of course, several other typical SRAM cells [3]–[8] are also proposed for low-voltage applications. However, most of these new SRAM cells, including the SE-8T cell, suffer from the half-select disturbance. In other words, they are not able to support the bit-interleaving (as well as called column selection) architecture which is extensively

utilized in SRAMs to afford soft error immunity in combining with the error correction code [9]. Therefore, some bit-interleaving-enabled SRAM cells are preferred to be adopted in the SRAM design. The representative one is the differential 10T (Diff-10T) bitcell [10]. It uses row-wise and column-line assists to form the cross-point configuration to eradicate the half-select problem together with the read destruction. Nevertheless, this bitcell circuit has more transistors, introducing remarkable area overhead. To make the matter worse, its write performance and write noise margin (WNM) are seriously exacerbated by the existence of the series-connected write access mechanism. Although the area cost is completely acceptable in advanced ultradeep-submicrometer regions, the poor write ability imparts a limitation on V_{DDmin} .

In this brief, we present a 65-nm 5.5-kb 10T SRAM based on an SE-10T SRAM cell. It characterizes the bitline-shared data-aware write assist to enable the column-selection structure. We also propose a Diff-VDD scheme to guarantee adequate WNM in the low-voltage environment. Moreover, a dropped-VDD biasing technique is used for power reduction.

II. PROPOSED 10T SRAM CELL WITH ASSIST

The original SE-10T SRAM cell of the proposed bitcell is shown in Fig. 1. A 4T read port composed of an inverter and a transmission gate (TG) is added to the 6T cell, isolating the read path from internal storage nodes. The inverter (M6 and M7) is driven by node QB and drives the read bitline (RBL) through TG (M8 and M9) which is controlled by two complementary read wordlines (WLs). This SE-10T cell can fully charge or discharge RBL by itself during a read operation. Thus, it is totally unnecessary to prepare a precharge circuit for RBL. The dynamic power is consumed on RBL just when the read datum is changed. That is to say, the dynamic power dissipation on RBL is zero if consecutive “0”s or consecutive “1”s are read out. This feature makes it suitable for video processing since image data have the special correlation, and similar data are read out in consecutive cycles [11]. Unfortunately, due to its 6T-like write operation, when initiating a write in a column-selection array, unselected cells in a row (or called half-selected cells) on the selected WL perform dummy read which indicates that the cells just undergo a read behavior rather than readout during a write operation, thereby experiencing the storage node upset similar to read disturb in the 6T cell. In other words, it is not eligible for the bit-interleaving architecture. In addition, the full rail-to-rail swing occurred on RBL congenitally dissipates more power compared with the differential readout. Meanwhile, bitlines incur more leakage current because of TG.

This SE-10T cell has been presented in [11]. However, our proposed 10T (thereafter called P-10T) circuit topology is different from the earlier design. Fig. 2 shows the P-10T based on the SE-10T cell. It exhibits improvements in the following aspects compared with the previous circuit.

First of all, the bitline-shared data-aware scheme is adopted to enable the column-selection architecture. In Fig. 2, the 6T part of the SE-10T cell is motivated by the y-direction (column direction) WL [column WL (CWL)]. In addition, two additional access transistors (M10 and M11) are added to connect the 6T cell, which

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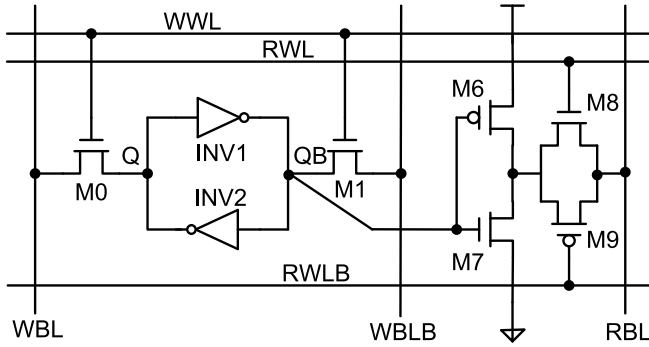


Fig. 1. Schematic of the SE-10T SRAM cell.

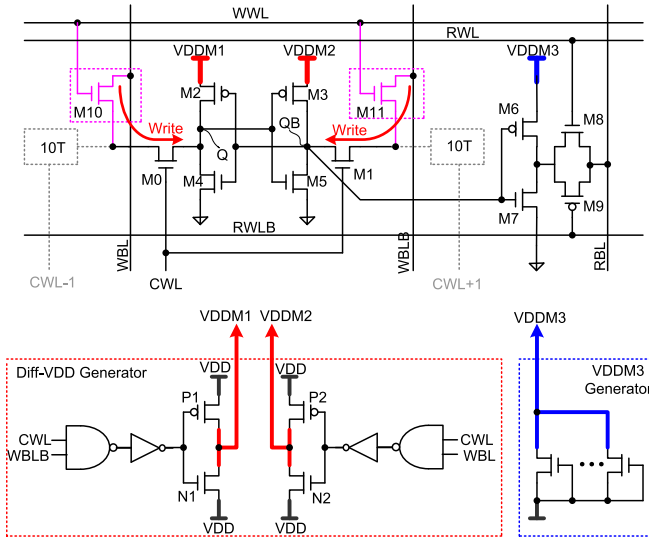


Fig. 2. Proposed SE-10T SRAM cell with assistant circuits.

are activated by the x -direction (row direction) write WL (WWL) and at the same time are powered by a complementary write bitline pair (WBL and WBLB). Every extra access transistor and write bitline are shared by two adjacent 10T cells in a row. During a write operation, the data are written into the storage core from shared write bitlines via shared access transistors and internal access transistors, just when row WL and column WL are all switched ON. The proposed bit-interleaving-enabled scheme is different from the previous design in [12] where the SRAM array is also able to be column-interleaved by vertical and horizontal WLs. Nonetheless, its write access devices are shared by several bitcells in a column, whereas the write access ones are shared by two bitcells in a row in our design.

Second, a Diff-VDD strategy is utilized to ameliorate the cell's write ability. We can observe from Fig. 2 that the power supplies of the 6T cell are coupled to two different virtual power lines (VDDM1 and VDDM2) produced by the Diff-VDD generator. Therein, VDDM1 is generated by ANDing CWL and WBLB to drive a power-ON inverter, in which the source terminals of pMOS and nMOS are all connected to VDD. Similarly, VDDM2 is obtained by ANDing CWL and WBL to drive the other power-ON inverter. These two VDDM lines are dropped differentially according to the values of the required written data. VDDM1 line is dropped at a write access for a "0" datum on WBL (WBLB = 1), while VDDM2 line is inversely dropped for a "1" write access.

Finally, we employ a dropped-VDD biasing for the read port, resulting in utterly noticeable power reduction. As shown in Fig. 2, the power supply of the 4T read port is biased over a virtual power line VDDM3 which is produced through several diode-connected

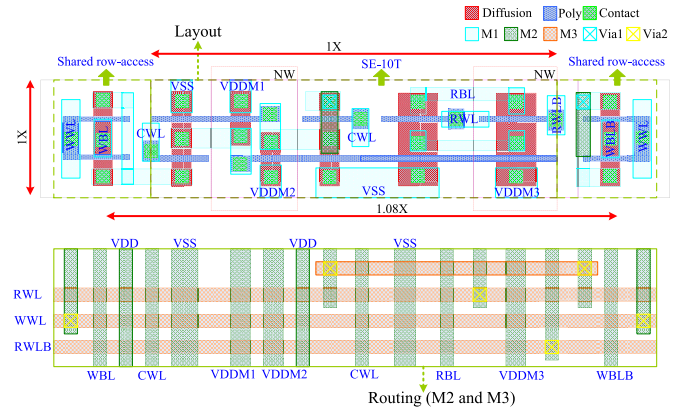


Fig. 3. Layout view of the cell and the arrangement of the signals.

TABLE I
PROPERTY COMPARISONS OF BITCELLS

	6T	SE-8T[2]	Diff-10T[10]	SE-10T[11]	This
Read-disturb free	×	√	√	√	√
Write ability	→	↑	↓	↑	↑
Bit-interleaving	√	×	√	×	√
Half-select issue	√	√	×	√	×
Non-precharge	×	×	×	√	√
Normalized area	1x	1.3x	2.1x	2.47x	2.67x

nMOSs. In general, a voltage drop (equal to V_{thn} approximately) is established across these diode-connected nMOSs, making RBL swing decline to $VDD - |V_{thn}|$. Consequently, much power saving is attained for a read operation. Normally, the values of the VDDM1, VDDM2, and VDDM3 all equal to approximately 0.75 V at $VDD = 1.0$ V in this design in a 65-nm CMOS, while the value of 0.39 V is obtained at $VDD = 0.5$ V. Admittedly, the power drivers of these three virtual power lines also introduce area overhead. It is estimated that less than 5% area contribution to the total array area is achieved for the drivers.

Fig. 3 shows the cell layout view and the arrangement of WLs, bitlines, and power lines. Since the row-access devices are shared by two adjacent SE-10T cells, the average area per P-10T is just increased by 8% compared with SE-10T. To relax the routing congestion, WLs except the CWL traverse the cell with M3 while other signals run vertical on M2. Besides, global power rails are inserted between two signals or virtual power rails on purpose, and long signal wires in parallel are avoided, mitigating the influence from the crosstalk noise.

The property comparisons of several typical bitcells are tabulated in Table I. For the SE-8T cell, it exhibits ample read stability and write ability without compromising much area overhead, but the bit-interleaving architecture is disabled owing to its 6T-like write mode. The SE-10T cell has the same properties as that of the SE-8T cell except the non-precharge circuit and the inferiority of the area. As far as the Diff-10T cell is concerned, it addresses the problems of the read disturb and half-selection but with the write ability and area sacrificed. Comparatively, the P-10T cell acquires these features only at the cost of the extra area.

A. Column-Selection-Enabled Array Architecture

To illustrate the column-selection-enabled capability of the proposed design, a matrix of 2 rows by 2 columns (2×2) as an example to describe the elementary write operational principle of the array is shown in Fig. 4.

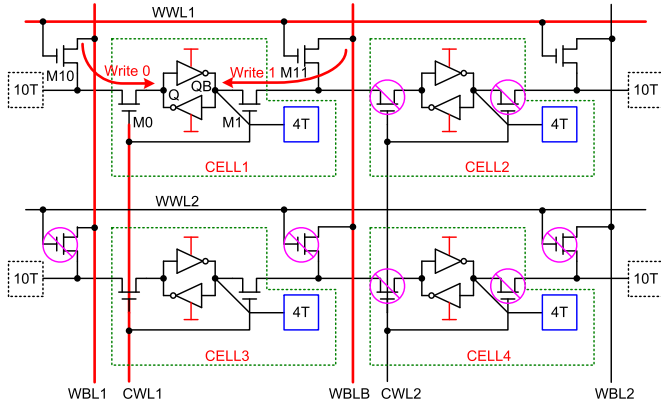


Fig. 4. Matrix of 2 × 2 with the proposed bit-interleaving architecture.

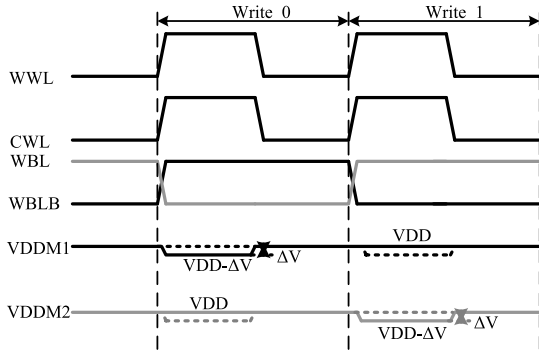


Fig. 5. Write waveforms of the P-10T cell.

Suppose the cell1 is chosen for write. The corresponding row WL WWL1 and column CWL CWL1 are switched ON, and the matched WBLs (WBL1 and WBLB) are charged or discharged depending on the data. If a “0” is expected to be written into the cell1, WBL1 is pulled down to low, and WBLB resides at high. As a result, storage node Q is discharged to “0” by access transistors M0 and M10. Then, the other storage node QB is pulled up to “1” through the internal cross-coupled feedback loop of the cell core. In the same manner, storage node QB is driven to “0” by access transistors M1 and M11 (WBL = 1 and WBLB = 0), and node Q is charged to “1” by the positive feedback loop, indicating a successful write “1.”

For the half-selected cell2, the state nodes are not perturbed during the write period, thanks to the CWL CWL2 switched OFF. Besides, the other half-selected cell3 holds its states since the row WL WWL2 remains at low, notwithstanding CWL1 ON. Overall, the proposed 10T SRAM array can assure the half-selected cells half-select-disturb-free regardless of in a row or in a column.

B. Diff-VDD Write Assist

The proposed design utilizes the row and column coordination modes of WLs to eliminate the half-selection problem, which leads to the degradation in the write ability due to the series-connected write access nMOSs just like in the Diff-10T cell. This could be highly problematic, particularly in the slow nMOS fast pMOS (SNFP) corner, where the driven strength of nMOS is less than that of pMOS. To solve this issue, the Diff-VDD scheme (shown in Fig. 2) is presented. Fig. 5 shows the write waveforms of the cell to describe the write assistant circuit how to work.

Generally, VDDM1 and VDDM2 are all equivalent to VDD because the pMOSs P1 and P2 in the Diff-VDD generator (Fig. 2)

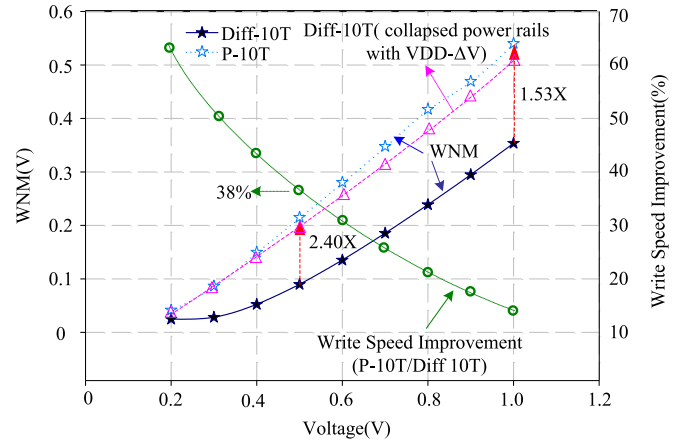


Fig. 6. WNM and write speed comparisons between Diff-10T and Diff-10T with collapsed VDD and P-10T. (All the results are simulated in a 65-nm process.)

are both turned on (CWL = 0). During a write “0” operation, WLs WWL and CWL are turned on, while bitline WBL is set to low and WBLB goes to high. Subsequently, the nMOS N1 is ON (CWL and WBLB = 1), resulting in a ΔV voltage drop on VDDM1. At this time, VDDM2 resides at VDD since CWL ANDING WBL equals 0. The dropped VDDM1 is able to attenuate the pull-up strength of pMOS M2 effectively, making the cascaded access nMOSs M0 and M10 absolutely pull the storage node Q down to “0.” Under the same condition, WBL goes to high, and WBLB is driven to low initiate a write “1” behavior. Similarly, a reduction of ΔV on VDDM2 power rail (CWL and WBL = 1) undermines the pull-up strength of pMOS M3 to ensure that the node QB can be discharged to “0” definitely by M1 and M11. The proposed Diff-VDD exerts a prominent advantageous impact on the write ability, facilitating the write operations.

Fig. 6 shows the comparison of WNM and write speed of the cells at the worst case scenarios (SNFP corner and 125 °C) at 0.5 V. As can be seen, the write ability of the Diff-10T with collapsed VDD is just slightly lower than that of the proposed design. But, thanks to the Diff-VDD technique, WNM of the P-10T cell achieves 1.53× higher than that of the Diff-10T cell at 1.0 V, while this value can be up to 2.40× as voltage scales down to 0.5 V, thereby showing the superiority of the write ability. At this voltage, the proposed circuit percentage improvement in the write propagation delay as well.

Although the Diff-VDD write method can improve the write ability of the cell, the lowered VDDM rails pose a detrimental influence on the hold noise margin (HNM) of the half-selected cells in a column. Fig. 7(a) describes the butterfly curves of the cells and shows their HNM comparisons at the worst conditions (fast nMOS slow pMOS corner and 125 °C) at 0.5 V. Note that HNM is estimated graphically as the length of the maximum nested square inserted the butterfly curves. It can be observed that asymmetric voltage transfer curves are obtained in half-selected cells due to the dropped VDDMs. Conversely, the unselected cells provide an abundant HNM. Fig. 7(b) shows the Monte Carlo simulation results of the distribution of HNM of the compared cells with 10000 occurrences and 3σ at VDD = 0.5 V, SNFP corner, and 125 °C. The unselected cells have an HNM of $\mu = 152.59$ mV and $\sigma = 2.032$ which is almost closed to that of the Diff-10T. By comparisons, the half-selected cells just achieve an HNM of $\mu = 107.05$ mV and $\sigma = 0.734$, comparing unfavorably with Diff-10T. However, this value is completely tolerable under this circumstance.

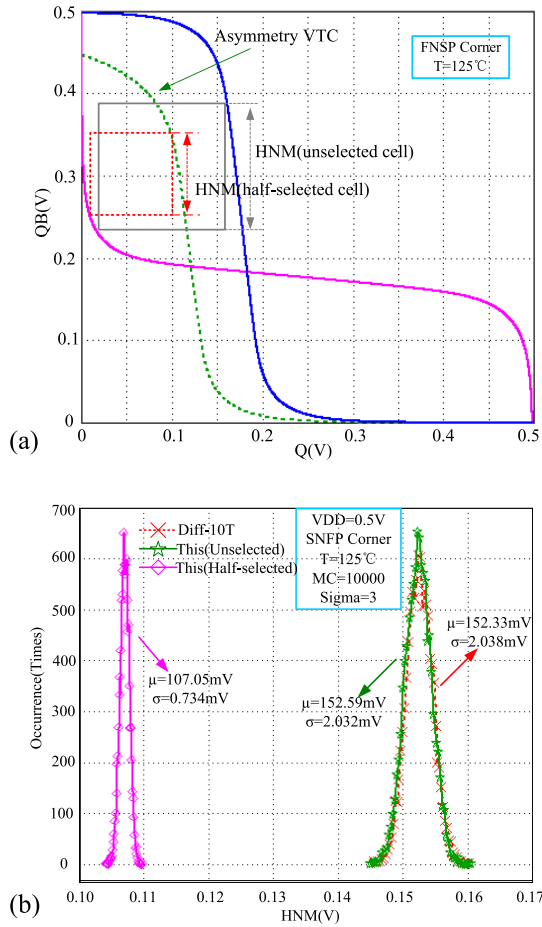


Fig. 7. (a) Butterfly curves of the unselected cell and half-selected cell at the hold mode. (b) Statistical distribution comparisons of HNM of the cells.

C. Dropped-VDD Power Rail

SE-8T SRAM usually uses a dynamic hierarchical bitline scheme for readout. It requires precharging circuits to charge the bitlines after read, introducing a vast amount of power. A 4T read port just like in SE-10T is utilized in our proposed design with non-precharging circuits. More importantly, we adopt the dropped-VDD technique to suppress the bitline swing, aggressively decreasing the power consumption. Of course, this would introduce 16% and 10% delay degradations in read “0” and read “1.” Fig. 8 shows the read path of the proposed 10T-SRAM. The power rails of the 4T read port of all cells in a column are furnished by VDDM3. A local bitline (LBL) attached eight bitcells is connected to a global bitline (GBL) via a first-stage tristate buffer (TSB), in which an inverter with low threshold (LVT) nMOS and high VT (HVT) pMOS is used to ensure that the reduced swings on LBL can be amplified. Next, GBLs are coupled to the second-stage TSBs controlled by the column-select signals.

Fig. 9 shows the read power consumption comparisons of SE-8T SRAM and SE-10T SRAM and the proposed design at VDD = 1.0 V and VDD = 0.5 V. (Assume that 128 cells are fixed on a GBL, and random read data are considered.) As can be seen, our proposed SRAM achieves 70.9% and 53.6% reductions in terms of the bitline dynamic power consumption at 1.0 and 0.5 V compared with SE-8T SRAM, while shows 45.1% and 33.3% saving compared with SE-10T SRAM, respectively, signifying pronounced improvement in the power dissipation.

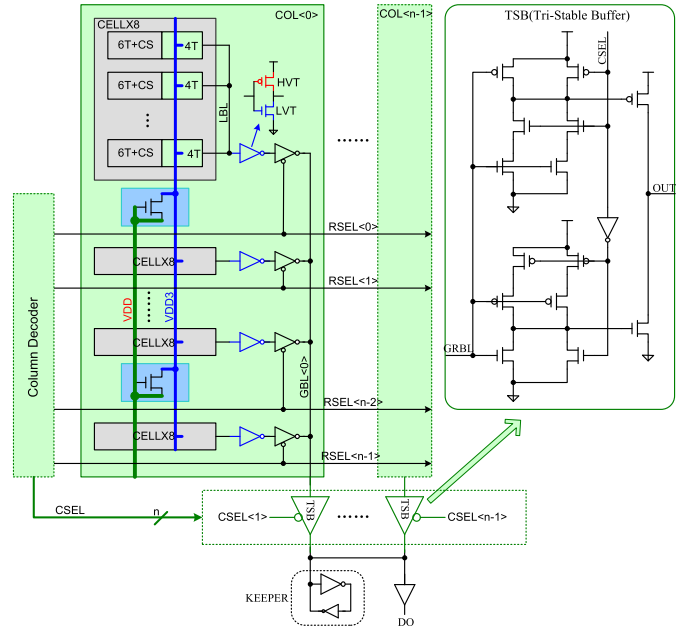


Fig. 8. Read path of the proposed SRAM.

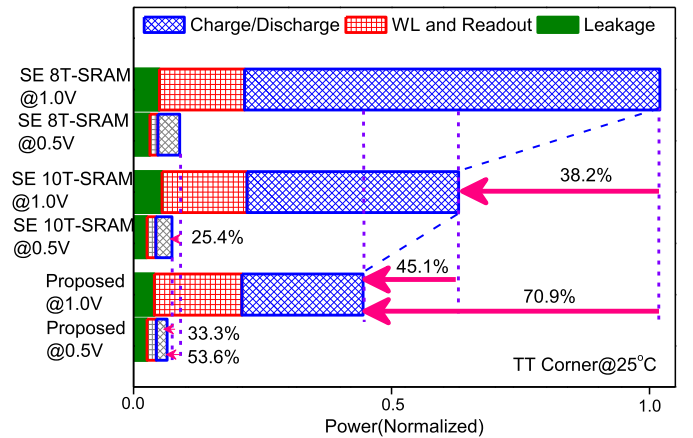


Fig. 9. Read power comparisons of SRAMs considering random data.

III. SRAM ORGANIZATION AND EXPERIMENTAL RESULTS

A 5.5-kb P-10T SRAM is implemented in a TSMC 65-nm CMOS. The layout view and SRAM organization are shown in Fig. 10. The SRAM array consists of 128 rows and 44 columns. (Number 4 is chosen for the column number.) Each column has independent power rails individually encompassing VDDM1, VDDM2, and VDDM3. In addition, virtual power drivers are distributed in the array well proportionately to guarantee the stationarity of VDDMs. It has a size of $235.6\text{ }\mu\text{m} \times 212.2\text{ }\mu\text{m}$.

Table II summarizes the experimental results of the proposed SRAM, and Fig. 11 shows the comparison of the power consumption between SE-10 SRAM and P-10T SRAM. As can be observed, the P-10T SRAM achieves a frequency of 6.25 MHz at 0.5 V even at slow nMOS slow pMOS corner, 125 °C, which is mainly determined by read “1” operation owing to the large bitline charging delay. It is worth noting that the energy consumption of read “0” is evidently larger than that of read “1.” Again, it has a total power of $62.25\text{ }\mu\text{W}$, in which $41.8\text{ }\mu\text{W}$ is leakage power, namely, dynamic power just occupies a secondary fraction of the total power benefiting from the presented techniques. Furthermore, the proposed design

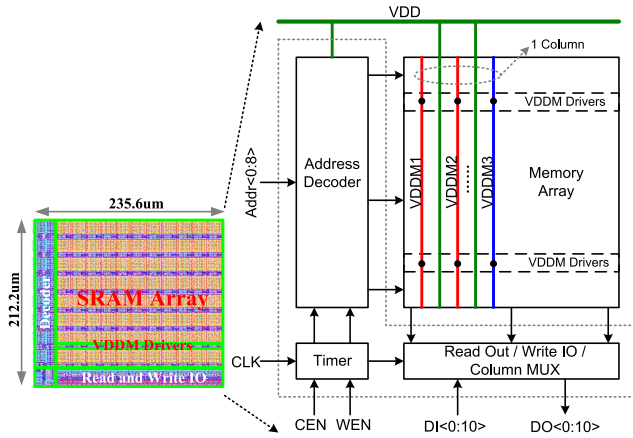


Fig. 10. Layout and organization of the proposed SRAM.

TABLE II
EXPERIMENTAL RESULTS OF THE PROPOSED SRAM

Technology	TSMC 65nm CMOS
Memory Capacity	5.5kb (512×11)
Memory area	49994.3μm ²
Frequency	6.25MHz@0.5V, SS corner, 125°C
Read “0” energy consumption	8.01pJ@0.5V, TT corner, 25°C
Read “1” energy consumption	7.74pJ@0.5V, TT corner, 25°C
Leakage power	41.8μW@0.5V, TT corner, 25°C
Total power	62.25μW @0.5V, TT corner, 25°C

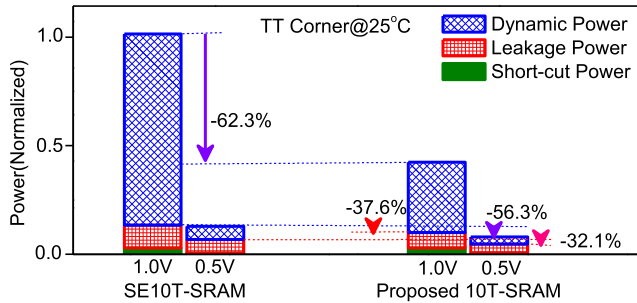


Fig. 11. Power comparisons between SE-10T SRAM and the proposed design.

shows 62.3% and 56.3% improvements in dynamic power as well as 37.6% and 32.1% reductions in leakage power at 1.0 and 0.5 V, respectively, compared with SE-10T SRAM, exhibiting superiority in the power consumption.

IV. CONCLUSION

A column-selection-enabled SE-10T SRAM is presented in this brief. The bitline-shared data-aware scheme and Diff-VDD are employed to enable the bit-interleaving and improve the write ability of the cells. Moreover, a dropped-VDD technique for power reduction is also proposed. The experimental results show that a 5.5-kb P-10T SRAM in a 65-nm CMOS achieves $3.3\times$ improvement in the write margin, together with 56.3% reduction in dynamic power dissipation and 32.1% saving in leakage power consumption compared with previous works, respectively.

REFERENCES

- [1] B. H. Calhoun and A. Chandrakasan, "A 256kb sub-threshold SRAM in 65nm CMOS," *IEEE ISSCC Dig. Tech. Papers.*, Feb. 2006, pp. 2592–2601.
- [2] L. Chang *et al.*, "Stable SRAM cell design for the 32 nm node and beyond," in *Symp. VLSI Technol. Circuits Dig. Tech. Papers*, Jun. 2005, pp. 128–129.
- [3] K. Takeda *et al.*, "A read-static-noise-margin-free SRAM cell for low-VDD and high-speed applications," *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 113–121, Jan. 2006.
- [4] T. Suzuki, H. Yamauchi, Y. Yamagami, K. Satomi, and H. Akamatsu, "A stable 2-port SRAM cell design against simultaneously read/write-disturbed accesses," *IEEE J. Solid-State Circuits*, vol. 43, no. 9, pp. 2109–2119, Sep. 2008.
- [5] L. Wen, Z. Li, and Y. Li, "Single-ended, robust 8T SRAM cell for low-voltage operation," *Microelectron. J.*, vol. 44, no. 8, pp. 718–728, 2013.
- [6] M.-H. Tu *et al.*, "A single-ended disturb-free 9T subthreshold SRAM with cross-point data-aware write word-line structure, negative bit-line, and adaptive read operation timing tracing," *IEEE J. Solid-State Circuits*, vol. 47, no. 6, pp. 1469–1482, Jun. 2012.
- [7] B. Wang, T. Q. Nguyen, A. T. Do, J. Zhou, M. Je, and T. T. H. Kim, "Design of an ultra-low voltage 9T SRAM with equalized bitline leakage and CAM-assisted energy efficiency improvement," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 2, pp. 441–448, Feb. 2015.
- [8] N. Maroof and B.-S. Kong, "10T SRAM using half- V_{DD} precharge and row-wise dynamically powered read port for low switching power and ultralow RBL leakage," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 25, no. 4, pp. 1193–1203, Apr. 2017.
- [9] S. Baeg, S. Wen, and R. Wong, "SRAM interleaving distance selection with a soft error failure model," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 4, pp. 2111–2118, Aug. 2009.
- [10] I. J. Chang, J.-J. Kim, S. P. Park, and K. Roy, "A 32 kb 10T sub-threshold SRAM array with bit-interleaving and differential read scheme in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 650–658, Feb. 2009.
- [11] H. Noguchi *et al.*, "Which is the best dual-port SRAM in 45-nm process technology? – 8T, 10T single end, and 10T differential –," in *Proc. IEEE Int. Conf. Integr. Circuit Design Technol. Tutorial*, Jun. 2008, pp. 55–58.
- [12] L. Wen *et al.*, "Bit-interleaving-enabled 8T SRAM with shared data-aware write and reference-based sense amplifier," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 7, pp. 643–647, Jul. 2016.